18.3 A 0.03mm² 9mW Wide-Range Duty-Cycle-Correcting False-Lock-Free DLL with Fully Balanced Charge-Pump for DDR Interface

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The DDR interface (I/F) technique is getting more important for memories, display drivers, communications, and other devices. For mobile systems, small area and low power consumption are especially required and single-ended signal transmission is preferred to reduce complexity of line patterns on the system board.

The issues of the conventional analog DLL for DDR I/F that consists of phase detector (PD), charge pump (CP), and voltage-controlled delay circuit (VCD) are as follows; 1) Trigger timing controlled by phase shifting of 90˚ and 270˚ is not always the best when the clock duty cycle degrades for a single-ended signal transmission. 2) There is a risk of false lock caused by initial condition of VCD. The essence of the false lock is that there is no distinction between non-harmonic and harmonic delays. 3) Metastability of PD inherently causes a two-cycle pattern on the control voltage of VCD which then causess the pattern jitter. Thus, the area of the filter will be larger to keep the pattern jitter smaller.

In order to address the above issues, the design concepts of the proposed DLL are as follows: Firstly, two sub-DLL structures are employed to generate rising edges (trigger timing) at the center of both high and low durations of the input signal. Secondly, a VCD scheme is proposed, in which only the falling edge is controlled. Thirdly, a PD scheme is proposed, in which the control voltage of VCD has only one cycle pattern. Thus, an accurate CP scheme named fully balanced charge pump (FBCP) is proposed to realize the above concepts.

Figure 18.3.1 shows the block diagram of the proposed DLL that consists of a single-ended to differential signal converter, two sub-DLLs (DLL1 and DLL2), an AND circuit, and a divide-by-two circuit. At first, single-ended clock (CLKi) is converted to two differential signals CLK and $\overline{\text{CLK}}$. Each sub-DLL performs locking behavior by its negative feedback loop that consists of a PD, an FBCP, and a VCD. In stable state, each low durations of $\overline{\text{UP}}$ and $\overline{\text{DN}}$ pulses is accurately controlled to be a half of high duration of the each input signal, respectively. The AND circuit combines $\overline{\text{UP}}_1$ and $\overline{\text{UP}}_2$ into a clock pulse (CLKdll). CLKdll is sent to the divide-by-two circuit then the triggered signal (CLKc) becomes the clock of 50% duty-cycle ratio.

PD performs the feedback control to make low durations of $\overline{\text{UP}}$ and $\overline{\text{DN}}$ equal. As shown in Fig. 18.3.1, $\overline{\text{UP}}_1$ ($\overline{\text{UP}}_2$) becomes low to discharge FBCP in the span from the rising edge of CLK ($\overline{\text{CLK}}$) to the falling edge of $\overline{\text{CLK}}_{d1}$ ($\overline{\text{CLK}}_{d2}$). On the other hand, $\overline{\text{DN}}_1$ ($\overline{\text{DN}}_2$) becomes low to charge FBCP in the span from the falling edge of $\overline{\text{CLK}}_{d1}$ ($\overline{\text{CLK}}_{d2}$) to the falling edge of CLK ($\overline{\text{CLK}}$). This type of PD inherently has no pattern jitter, because it outputs both $\overline{\text{UP}}$ and $\overline{\text{DN}}$ within one CLK period, which contributes to area reduction.

Figure 18.3.2 shows the block diagram of the proposed FBCP that is the key technology to balance charge and discharge. Transistors of current sources and switches (M_1, M_2) have the same polarity and size, respectively. M1 (M2) pumps pull current (push current) when $\overline{\text{UP}}$ ($\overline{\text{DN}}$) is low. M_3, M_4, C1, and AMP1 configure the charge copier that converts the pull charge (Q_{UP}) to the filtered current ($Q_{UP(DC)}$: dc in the simplified case) by C1. The active filter (AMP2 and C2) with the output Vc integrates periodic push charge (Q_{DN}) minus $Q_{UP(DC)}$. Vc returns to a certain fixed voltage within one period in stable state, thus, the proposed scheme generates no pattern jitter. The percentage of the low durations of $\overline{\text{UP}}$ and $\overline{\text{DN}}$ depends on the equality between push and pull charges. Virtual shorting at node A and B makes the equality between Q_{UP} and Q_{DN} very high including noises such as switching feed through, charge injection, drain leakage, and junction leakage (see Fig.18.3.3). Virtual shorting also makes the equality between periodic Q_{UP} and $Q_{UP(DC)}$ very high in stable state. Thus, the FBCP achieves higher accuracy than other single-ended type CPs [1]. The merit of the charge copier appears in the rising gradient of Vc, which is smaller than that of a mere current mirror. Suppressing rising gradient makes delay variation of VCD smaller. The minimum supply voltage is approximately defined by one threshold voltage + two drain-source saturation voltages. It is lower than other type of CP. Moreover, the FBCP is robust against PVT variations because of its highly symmetric structure.

Figure 18.3.4 shows the block diagram of the proposed VCD. Since simultaneous delay of both rising and falling edges causes the harmonic lock, the VCD delays only the falling edge of $\overline{\text{CLKI}}$ by Vc and M_6. $\overline{\text{CLKI}}$ is led to the hysteresis circuit (INV2 and M_9) to prevent chattering. The delay time (td) is defined by sum of delay from INV1 to INV3. The maximum td is limited by a bias voltage (Vbias) and M_8. The only one delay-stage in the VCD results in low power consumption.

The proposed DLL is fabricated in a 0.3µm CMOS process (See Fig.18.3.7). The active area is 0.03mm² without a reference generator. The target specification of the prototype is as follows: frequency range is from 20MHz (=40Mb/s/pin) for display devices to 300MHz (=600Mb/s/pin) for memory I/F, and supply-voltage range is from 2.0V to 4.0V for compatibility with conventional systems.

Figure 18.3.5 shows measured waveforms at 40MHz, 30% duty-cycle ratio, and V_{DD}=3.0V. CLKi(delayed) is a delayed signal of CLKi by a replica delay circuit. It is confirmed that CLKdll has rising edges at the center of high and low durations and the duty-cycle ratio of CLKc is corrected to 50%. Figure 18.3.5 also shows the evaluated overall performances of this work. The center offset means the offset from the center point of high or low durations. Plus value implies that trigger timing is faster than the true center and minus one means opposite case. Estimated center offsets are in the narrow range from –14.5ps to +12.5ps. Duty-cycle ratios of 49% to 51% are achieved in spite of degrading by PVT variations.

Figure 18.3.6 shows a comparison to recent works of near process generations or near targets; an analog type [2], a digital type [3], and a dual-loop type [4]. It is confirmed that this work not only has comparable frequency range and jitter performance, but also wider V_{DD} range, lower power consumption, and lower area with duty-cycle correction and false lock free functionality.

Acknowledgments:
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References:
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[4] E. Song, et al., “A Reset-Free Anti-Harmonic Delay-Locked Loop Using a Cycle Period Detector,” *IEEE J. Solid-State Circuits*, vol.39, no.11, pp. 2055-2061, Nov., 2004.

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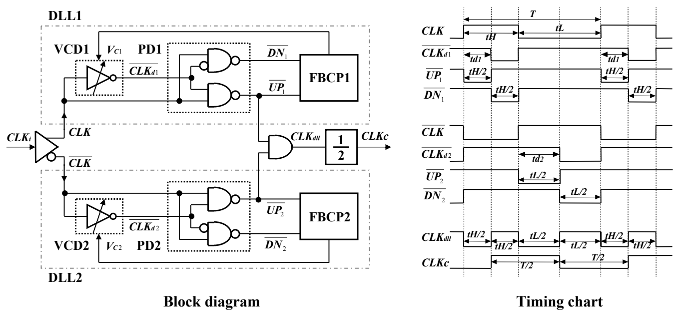


Figure 18.3.1: Proposed DLL circuit.

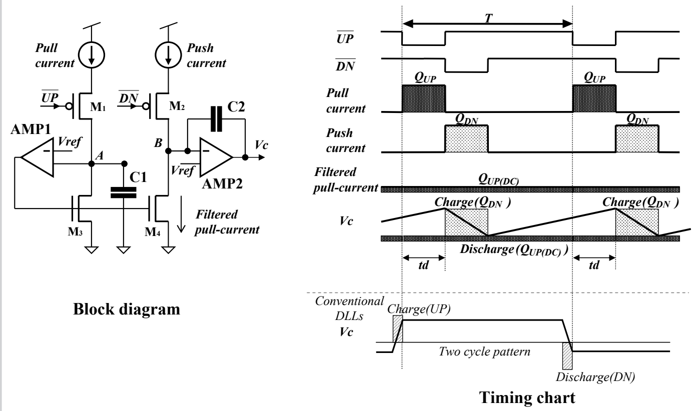


Figure 18.3.2: Fully balanced charge-pump circuit.

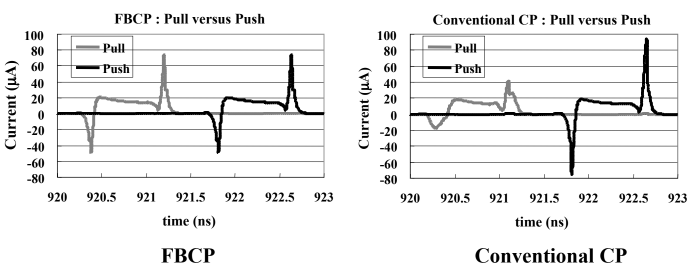


Figure 18.3.3: Simulated waveforms of pull and push currents at 300MHz.

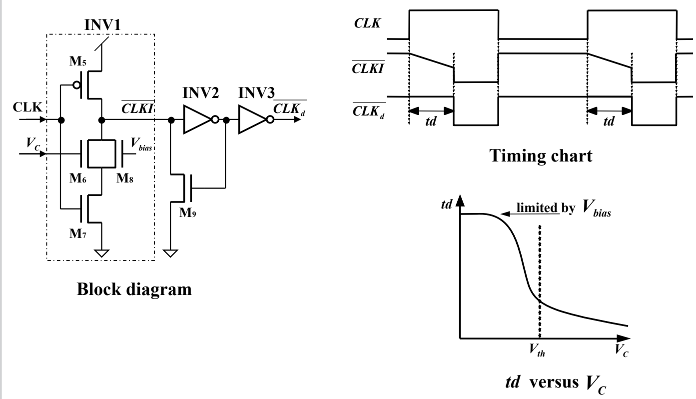
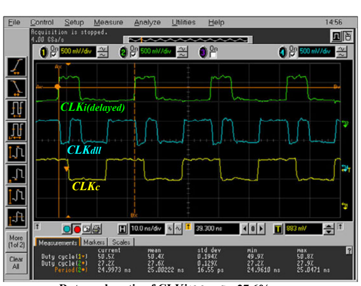


Figure 18.3.4: Voltage-controlled delay circuit.



Duty cycle ratio of CLKi(delayed) : 27.6%
Duty cycle ratio of CLKc : 50.4%

Measured waveforms@40MHz

Process	0.30μmCMOS
V_{DD}	2.0V - 4.0V
Freq .range	20 MHz - 300 MHz
Input duty range	30% - 70%
Center offset	-14.5ps - +12.5ps
Output duty range	49.6% - 50.5%@20MHz 49.0% - 51.1%@200 MHz 49.0% - 50.9%@300 MHz
Period Jitter	98.6ps@20MHz 6.9ps@200 MHz 5.7ps@300 MHz
Power consumption	9mW @300 MHz (with Ref .Gen)
Locking time	1.8μs
Area	0.03 mm 2 (DLL only) 0.09 mm 2 (with Ref. Gen .)

Performance of this work

Figure 18.3.5: Evaluated performances of this work.

	This work	Y. Moon [2]	T. Hamamoto [3]	E. Song [4]
Type	Analog	Analog	Digital	Dual Loop
Process	0.30μm CMOS	0.35μm CMOS	0.13μm CMOS	0.25μm CMOS
Area	$0.03\,mm^2$ *1	$0.20\,mm^2$	$0.25\,mm^2$	$0.66\,mm^2$
VDD	2.0V - 4.0V	3.3V	1.7V - 1.9V	2.5V
Frequency Range	20M-300MHz	62.5M-250MHz	200M-333MHz	30M-200MHz
Period Jitter	6.9ps @200MHz	4ps @250MHz	11.2ps @200MHz	7.1ps @200MHz
Power Consumption	9mW *2 @300MHz	41.6mW @250MHz	21.4mW @333MHz	30mW @133MHz
Duty Cycle Correction	Yes	Yes	No	No
Input Duty Cycle Ratio	30% - 70%	-	-	50%
Output Duty Cycle Ratio	49% - 51%	49% - 51%	-	-
False Lock Free	Yes	Yes	Yes	Yes
Immunity to Duty degradation	Yes	No	No	No

*1 $0.09\,mm^2$ including Ref.Gen.
*2 at V_{DD} =3.0V

- no description.

Figure 18.3.6: Performance comparison.

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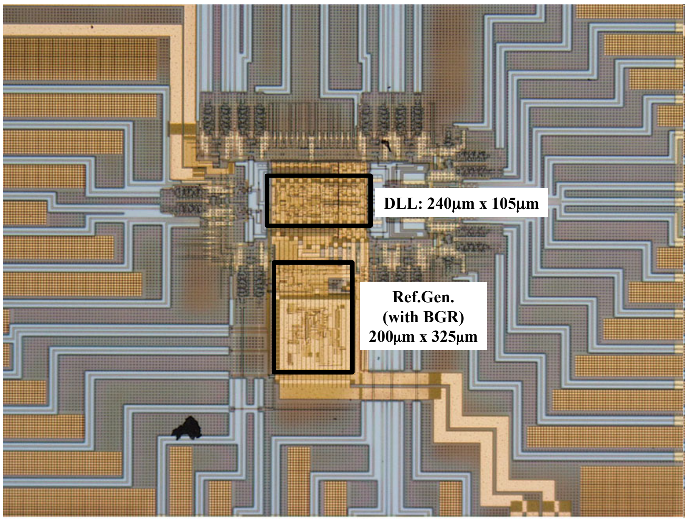

Figure 18.3.7: Die micrograph.

